A Study and Comparison of Different Types of SRAM Designed for Usages with Low Power Consumption

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ABSTRACT: Today, with the development of the semi-conductive devices building technology, the speed and power consumption parameters play a major role in increasing the electronic devices capability and speed. Because the electronic chips with high speed and low power consumption have always been the favorite choice for the military industries and research and commercial centers. The elite group of scientists and chip designers in chip making companies such as Intel, IBM and Soltra advanced all their activities towards making high-speed chips with high capabilities and low power consumption rate. The electronic systems are made up of two parts, namely analogue and digital. The digital systems are bigger and bulkier. Therefore, they are more decisive in the designing competition. When designing the digital systems, various parameters such as the chip performance, power consumption, leaking current and supply voltage are of significant importance. On the other hand, the SRAM memories are considered as one main part on the SOCs circuits. This type of memories does not require information readouts. Thus, their speed is considerably higher than the dynamic memories. Therefore, the static memories are fast and expensive. Static memories are utilized for building the microprocessor Cache memories (speed-sensitive). The SRAM memories waste a considerable amount of power consumption (roughly 45%) in computer systems. Hence, the power consumption reduction techniques should be considered when designing the SRAM memories. In this paper, first various cells which were designed and proposed to date are studied in terms of stability and power consumption. Second, the existing challenges regarding these cells are indicated. Then, the designed cells power consumption is studied in various technologies.

Keywords: Memory blocks, SOCs circuits, SRAM memories, power consumption, leaking current

1. INTRODUCTION

Today, the increasing growth of using portable electronic devices such as the wireless telecommunication systems, portable multimedia devices and/or the sensitive medical equipments with low-power circuits received a lot of attention more than ever before. This led to so many efforts to be made in the direction of building low-power circuits regarding which the manufacturers compress more memories and logical circuits intoa single chip. Scientists believe that a new model of the chip industry is being formed in which new combinations of memories and logical circuits exist and they ultimately lead to the widemmanufacture of new processors with different and new memory architectures. The static memory has also received a lot of attention as a main block in SOCs circuits. In fact, the static memories are designed to meet two main objectives (Kr. Shukla, 2011):
1- Providing a direct connection with CPU (since the dynamic memories cannot satisfy this need in higher speeds).
2- Replacing the dynamic memories due to their high power consumption.

The large number of transistors employed in these memories and also the high leaking current rate with regards to the advances in technology caused these circuits to be recognized as the high density circuits. Then, it was attempted to reduce the power consumption rate by reducing the input power supply (Kr. Shukla, 2011).

In recent years, designers tried to reduce the power consumption rate in these memories by reducing the input power supply. But, the data stability will reduce accordingly due to this reduction. (Various designers try to build and design circuits with higher stability and the least power consumption rate.) Regarding the fact that more power is spent on the data stability in the DRAM memories compared to the SRAM memories, they have higher...
performance in portable devices with static memories. The access time is roughly the same in both the static and dynamic memories. (The access time is the interval between the reading start and the appearance of the output data). [Shukla, 2011]

In this research, the concepts related to the memory architecture, the SRAM cell, power consumption and its related reduction techniques are presented in sections 2 and 3. Then, various cells that have been utilized for designing and suggesting the SRAM memories to date are introduced. Finally, their power consumption rates in various technologies are compared with one another.

2- The Memory Architecture

2-1 The Classification of Memory

The electronic memories are made in various types and forms. The type of memory that a specific user needs is a function of the required number of memories, the access time for reaching the stored data, how to access, usage and system requirements (GM. Sreerama, 2009).

The required time for memory readouts is called the access-readout time that is equal to the delay between the reading request and the time when the data is being prepared in the output. This time is different from the access-readout time that is the spent time between the reading request and writing the input data in the memory. Another important parameter is the cycle time (read or write) that is the least required time between the consecutive reading and writing.

The final classification of the semi-conductive memories is done based on the number of input and output ports that are shown in table 1, namely the classification of the semi-conductive memories (Jan M. Rabaey. 1996).

<table>
<thead>
<tr>
<th>ROM</th>
<th>NVRWM</th>
<th>RWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmed with the programmable mask (PROM)</td>
<td>EPROM</td>
<td>FIFO LIFO</td>
</tr>
<tr>
<td></td>
<td>E1 PROM</td>
<td>Shift Register</td>
</tr>
<tr>
<td></td>
<td>FLASH</td>
<td>CAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SRAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRAM</td>
</tr>
</tbody>
</table>

3- SRAM Cell

The SRAM cell is considered as a main part in today’s SoCs circuits. In this type of memories, the Flip Flop II is used for storing each memory bit. A flip flop uses 4 to 6 transistors for one memory cell (Kr. Shukla, 2011).

The memory designers have always tried to present a new unique cell and/or a novel approach in setting cells in order to reduce the power consumption rate. Yet, the 6-transistor cell was the proper choice for reducing the power consumption rate in most cases. However, many designers built cells with much lower power consumption rates. In figure 1, a 6-transistor cell is shown. This circuit is composed of two inverters that are located back to back next to one another. Also, two nMOS transistors are utilized in this memory cell for contacting other circuits.

Figure 1: The Single Base Cell of the Static Memory Composed of 6 Transistors (Kr. Shukla, 2011)

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1 Flip Flop
In this memory cell, the M3 and M4 transistors are called the driver transistors. Their job is to discharge the BitLine when reading the data. The M1 and M2 transistors are also known as the access transistors. These transistors are employed along with other parts of the memory for building contact among the inverters. The gate related to these transistors is called WordLine. The M5 and M6 transistors are called the load transistors. Their internal nodes will have values 0 and 1 with respect to the value stored in the cell.

Generally, three main operations are done within these cells (Sheng Lin 2008).
- Data retention: The SRAM memory cell is able to retain the data as long as it is plugged to the power supply.
- Data reading: The cell can transfer the stored data properly to other units. The reading operation is nondestructive.
- Data writing: Values 0 or 1 can be set on the cell.

3-1 Various Types of the Designed SRAM Cells.

3-1-1 6T SRAM

In figure 2, the circuit structure of the 6-transistor cell is depicted. This type of cell forms the basis for all other cells. As it was mentioned earlier, the SRAM cell is made up of a latch that is located as an input and output bridge for those two control transistors (S. Birla 2010, B Zhai, 2007).

![Figure 2: The Circuit Structure of the 6-Transistor Cell (S. Birla 2010, B Zhai, 2007)](image)

3-1-2 6T Single-Ended cell

The 6-transistor cell with unique output was proposed by Hanson (B. Zhai, 2007) in 2007. In figure 3, this cell is shown. Compared to the conventional transistor cell, this cell has the quality of improving the stability at the time of reading. However, the SNMwrite noise safety margin will reduce as a result. In order to lessen this effect, the supply voltage will reduce at the time of writing. Therefore, the sudden drop in the supply voltage will improve with an increase in SNMwrite and also selecting the proper proportion \( \frac{1}{w} \) for the inverters and the transmission gate. As a result, the data will be retained in the transistors to which there is no access.
3-1-3 8T Dual-Port
One of the inherent problems posed by the conventional 6-transistor cells is the sudden increase in the voltage of one of the internal nodes at the time of reading. The cell that was suggested by (B. Zhai, 2007) will resolve this problem using a buffer for separating the reading operation from the writing operation. As is shown in figure 4, this 8-transistor cell has separate WLREAD and WLWRITE.

One of the significant qualities of this single cell is the optical tomography operation conducted on the conventional 6-transistor cell. In figure 4, the circuit structure of this base cell is shown (J. Suganthi, 2012).

3-1-4 10T with Reduced Bitline Leakage Cell
Due to the inherent reduction of SNMREAD in the 6-transistor cell and regarding the fact that a large number of cells on the BL line are common, the leaking currents originating from the off cells create a critical current that is comparable to the actual current. To tackle this problem, the 10-transistor cell was proposed by K. Daeyeon (2011). This cell is a solution for eliminating the inherent reduction of SNMREAD. Moreover, the leaking current was also
reduced in the off cells. Figure 5 shows the structure of this cell. As you can see in this figure, the WL and RWL are separated from one another to reduce the SNMREAD in a similar fashion to the 8-transistor cell.

![Figure 5: The Cell Structure Related to the Static Memory (K. Daeyeon, 2011)](image)

The problem raised with the presence of the leaking currents is resolved to a large extent by the usage of the STACK transistors. On the other hand, SNMWRITE will reduce as the virtual power supply connected to the PMOS transistors is being used and upon the reduction in this voltage at the time of writing (K. Daeyeon 2011).

### 3-1-5 10T with Bit-Interleaving Capability

In this cell, the efficiency and the SNM are improved using a simple technique. As the AL1 and AR1 transistors are added, which is controlled by the WWL, this cell provides easy access to every single cell at the time of writing. Similar to the 8-transistor cell, the reading process will not take place destructively in this cell. Therefore, there is no need to worry about the voltage change in the internal node. On the other hand, the increase in WL, VW and VWL voltages will lead to an increase in the launching power of the AR2 and AL2 transistors. As a result, the reading ability will increase without having to increase the size of the transistors. In figure 6, the structure of this circuit is shown (P.G. Scholar, 2013).

![Figure 6: The Structure of the 10-Transistor Cell Proposed by (P.G Scholar, 2013)](image)

### 3-1-6 10T Schmitt Trigger Based Cell

The cell depicted in figure 7 has an acceptable stability compared to the other proposed cells. Unlike other cells, there are two NMOS transistors in each inverter that lead to more reduction in the leaking currents. This cell has an explicit difference with other cells in terms of structure. The most conspicuous property of this cell is its application in large memories due to its low leaking currents (K. Daeyeon, 2011).
Figure 7: The Cell Structure Related to the Static Memory (K. Daeyeon, 2011)

4- The power consumption
The power consumption in CMOS circuits is the sum of the following two components (M. Sivamangai, 2011).

\[ P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} \]

Where, \( P_{\text{static}} \) and \( P_{\text{dynamic}} \) are the static and dynamic power consumptions, respectively. The static power refers to the leaking current or any other related current that is extracted continuously and steadily from the power supply. This loss is proportionate to the number of transistors in the system that is normally constant. Unfortunately, the more the transistor gate width increases, the more the pre-threshold current, the static power consumption, and even the static CMOS increase. Regarding the above description, the static consumption rate is obtained according to the following relation (Kr. Shukla, 2011):

\[ P_{\text{static}} = \sum_{i=1}^{n} (I_{\text{leakage},i}) \times V_{\text{DD}} \]

Where, \( n \) indicates the number of CMOS circuit transistors.

The dynamic power consumption refers to the power that is consumed when switching modes with regards to the signal change. This amount is concordant with the passage of the interruption-related transient flow, switching, and the load capacitors discharging according to the input changes. The power formula related to the dynamic power consumption is as follows (Kr. Shukla, 2011):

\[ P_{\text{dynamic}} = V_{\text{DD}}^2 \times C_{\text{load}} \times f \]

Where, \( V_{\text{DD}} \) is the supply voltage and \( C_{\text{load}} \) is the load capacitor that is charged or discharged during an evaluation phase. It includes the transistors capacitors and wires capacitor. \( f \) is the number of gate switching in the time unit. If the circuit switches mode per each clock period, \( f \) will equal the clock frequency. In this formula, the most important factor is \( V_{\text{DD}} \) (M. Sivamangai, 2011).

Besides the above power consumption, there also exists another power component related to the direct path (short circuit) for both n and p networks. It is created due to the rising and falling times of input signals. The short-circuit power consumption formula is as follows:

\[ P_{\text{SC}} = V_{\text{DD}} \times I_{\text{peak}} \times t_{SC} \times f \]

Where, \( I_{\text{peak}} \) is the saturation flow of the p, n networks that is proportionate to the transistors size. \( t_{SC} \) is the time interval when both networks are on during the mode change. Usually the power loss is ignored in the short circuits (Kr. Shukla, 2011).

Similar to other digital design areas, the reduction in power consumption is also another important priority. In portable applications, the maximum limit for power is constantly decreasing. However, the technology shrink and the decrease in the supply voltage and threshold and its destructive effect on the leaking current of the transistor cause the memories static power to increase (M. Sivamangai, 2011).
In order to reduce the power consumption in SRAM memories, we need to identify the factors that cause an increase in the power consumption. Then, we should study the necessary techniques for the power reduction. These techniques are (c. Bipul, 2006).

4-1 The Reduction of the Dynamic Power Consumption
Although the static power has had a significant increase in all generations of the SoCs circuits, the dynamic power still encompasses a large portion of the microprocessors power consumption. Therefore, various techniques and architectures are proposed for designing the circuits to reduce the dynamic power consumption. The most important technique is (c. Bipul, 2006):
- Optimization of the transistor size and the chip surface connections
- Clock Gating
- Optimization of the power supply

4-2 The Reduction of the Dynamic Power in SRAM
To speed up the reading process, the bitline voltage switching should decrease as much as possible. Usually 0.1 to 0.3 v resulting signal will connect to the measuring amplifier to be modified again. Since the signal results from the division of load between the online bit and the cell transistor, the current will flow in the bitline until the word is active. Limiting the and the bitline reduces the active power losses in SRAMs (c. Bipul, 2006). The reduction of the supply voltage has its effect on the memory access time. The reduction of the partitions threshold voltage is the only possible solution, providing we could control the resulting leakage increase especially in inactive cells (c. Bipul, 2006).

Regarding the tables, the resulting graphs and their related comparison, generally in high-scale technologies, the power consumption of various SRAM cells will decrease due to an increase in the channel length. Moreover, regarding the formula \( p_{\text{dynamic}} = V_{DD} \times C_{\text{load}} \times f \) regarding the power consumption, the power consumption will have a sharp decrease with a decrease in the power consumption channel width. Generally, the power consumption rates related to the pre-mentioned cells are shown in various technologies.

<table>
<thead>
<tr>
<th>cell</th>
<th>65nm</th>
<th>90 nm</th>
<th>130nm</th>
<th>180nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SrRam Cell</td>
<td>2.46810</td>
<td>1.99610</td>
<td>96.49320</td>
<td>0.00002</td>
</tr>
<tr>
<td>6T Single Ended SRAM Cell</td>
<td>0.00849</td>
<td>0.00376</td>
<td>0.01995</td>
<td>0.00002</td>
</tr>
<tr>
<td>8T Dual Port SRAM Cell</td>
<td>3.31690</td>
<td>2.31230</td>
<td>111.15090</td>
<td>0.00043</td>
</tr>
<tr>
<td>10T Schmitt Trigger SRAM Cell</td>
<td>2.23160</td>
<td>1.80320</td>
<td>59.10100</td>
<td>0.00002</td>
</tr>
<tr>
<td>10T with bit intervaling</td>
<td>18.86270</td>
<td>14.93870</td>
<td>118.28930</td>
<td>9.41520</td>
</tr>
<tr>
<td>10T With Reduced Bitline Leakage</td>
<td>5.04360</td>
<td>4.56400</td>
<td>61.94450</td>
<td>0.00009</td>
</tr>
</tbody>
</table>

Also in the following graph, a comparison of the presented cells power consumption rates are depicted in various technologies.
Graph 1: A Comparison of the Cells Power Consumption Rates in Various Technologies

As it can be seen from the above power consumption graph in various technologies, the power consumption rate related to the SRAM cells decreases in high-scale technologies. As a result, the power consumption rate decreases as the channel length in transistors increases and also due to a decrease in the channel resistance. According to the formula $I_d = \mu C_{ox} \frac{W}{L} V_{th} e^{\frac{V}{2V_s}}$, the more the channel length, the less the current per the threshold voltage and thus, the transistor will direct in lower voltages. Therefore, the power consumption rate will decrease accordingly. Hence, as is shown in graph 1, the least power consumption rate in 10T Schmitt Trigger cell is observed with the 180 nm technology.

5. Summary and Conclusion
In recent years, the increasing growth in portable electronic devices such as the wireless telecommunication systems, portable multimedia devices and/or even the sensitive medical equipments has required low-power circuits. This led to so many efforts to be made in the direction of building low-power circuits. In near future, the static memories will occupy roughly 60 percent of a chip. Regarding the trajectory of the technology advancements and due to the smaller sizes of the elements, the occupied memory volume has increased drastically. As a result, the reduction in the memories power consumption rates is one of the major challenges today. One solution is to reduce the supply voltage. But this decrease increases the circuit delay and PDP increases accordingly. The least PDP value occurs in the pre-threshold area. But this leads to a decrease in cell stability. Hence, additional circuits are required to increase the reliability. This means the used space and cost will increase as well. The important point here is the presence of a kind of compromise between the occupied space and the circuit efficiency.

Various memory designers have always faced challenges such as power consumption, occupied space, reliability and delay in receiving data. The key point in this case is that none of them can be adjusted with the other, i.e. when each of these parameters is improved, the possibility of failure in other parameters will increase significantly. Therefore, there has always been a kind of compromise in most cases.

In this project, first the static memories are reviewed and a few designed cells are introduced. Then their related properties and shortcomings are specified. Finally, their power consumption rates are compared with one another. Due to the fact that the transistors operate in pre-threshold areas, the static power is reduced quite tangibly. However, a few techniques, e.g. using transistors with transmission gates, are employed. In future, designers will direct all their efforts towards finding and suggesting a solution for more reduction in power consumption rate and designing cells with the least power consumption rates.

6. REFERENCES


