Design of a Low-Power Switched-Capacitor Bandpass Filter in 0.18µm CMOS Technology with Quality Factor Tunability

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ABSTRACT: In this paper, the design of low-power second-order switched–capacitor bandpass filter is presented in 0.18µm CMOS technology. Instead of two operational amplifiers in conventional structures only one operational amplifier is used to significantly reduce power consumption and chip area. Quality factor and maximum gain can be simply tuned by employing low-threshold NMOS transistors as the non-overlapping clock signals with the 1.2 volt amplitude and the period of 1msec to the switches without any variations in the central frequency. With the quality-factor tuning technique the central frequency is 300Hz and the quality factor for the selective values of capacitors is 0.54. The filter has the low power consumption about 0.59nW from a 1.2 supply voltage. In this design the NMOS operational amplifier which has the high gain for the purpose of decreasing gain error consumes 141µm² while the total chip area of the proposed circuit is 226µm².

Key words: Band pass filter, Low chip area, Low power, Quality factor tuning, Switched capacitor.

Abbreviations: Op-Amp- Operational amplifier, PLL- Phase locked loop, SC- Switched capacitor.

INTRODUCTION

Analog bandpass filters with low power consumption are used in many communication systems and cardiac pacemaker (Al-Badawy et al., 2009). In active RC-filters, the resistors are temperature dependent and consume large area, so they are replaced by the switched capacitor (SC) filters which are really sophisticated and accurate (Huang et al., 2010). They become increasingly popular for their advantages. Recently in the phase locked loop (PLL), the switched capacitor filters are used to decrease spur levels and jitters (Song and Ignjatovic, 2010). They are less sensitive to temperature changes and by changing clock signals their cutoff frequency can be tuned. The switched capacitor filters are the most suitable choice in integration circuits at the lower system cost. In such circuits when the switches are opened and closed, the capacitors can be charged and discharged. Non-overlapping signals are applied to each switch for controlling them. The charge is sampled on the capacitor so they work as analog sampled-data systems.

Ratios between the sizes of the capacitors in SC filters determine the central frequency, the quality factor and the maximum gain. The time constants in these circuits can also change by the ratios of capacitance and do not depend on the values of passive elements (Suzuki et al., 2010). One of the well-known second-order bandpass filters is Fleischer and Laker switched capacitor biquad cell. In such filters two operational amplifiers (Op-Amps) work with each other at any phase. Op-Amps produce noticeable power consumption. Thus traditional biquad circuits have more power dissipation. In (Lee et al., 2008) switched Op-Amp (SO) technique was proposed to solve this problem. In that modified SC biquad filter only one Op-Amp is active in each phase, without changing function of biquad filter.

Another solution is, using one Op-Amp instead of two. It is applied in implantable medical devices which needs low power consumption (Zade, 2008). In addition of the low power dissipation, the chip area and input referred noise of the filter are eliminated. The only problem which limits this technique for biomedical applications is low quality factor. Therefore in communication circuits, filters with two Op-Amps are used to achieve high quality factor. Sometimes external ceramic filters are used in several ultra high frequencies to increase quality factor (Oualkadi et
In this paper, a second-order bandpass filter with one Op-Amp is proposed based on 0.18µm CMOS technology. The quality factor tuning technique is used to achieve better performances, and solve the problem of one Op-Amp topology.

In section 2 second order SC filter with one Op-Amp is proposed. Section 3 introduces the way for improving the quality factor. Finally, the results are shown in section 4.

### Second-Order Single Op-Amp Filter

A bandpass filter is a device that has transfer function in the Laplace domain as follows:

$$H(s) = \frac{H_0(\frac{\omega_0}{Q})s}{s^2 + (\frac{\omega_0}{Q})s + (\omega_0)^2}$$

where $H_0$ is the maximum gain, $\omega_0=2\pi f_0$ is the central frequency and $Q$ is the quality factor of the filter. Using forward-Euler mapping, Laplace-domain can be changed into $Z$-domain. The relationship between $s$ and $Z$ is:

$$s = \frac{2}{T} \left( \frac{1-Z^{-1}}{1+Z^{-1}} \right)$$

where $T=1/f_s$, $f_s$ is the sampling frequency period. Hence the $Z$-domain transfer function of the filter is:

$$H(Z) = \frac{-H_0(\frac{\omega_0T}{Q})}{(1-\frac{\omega_0}{2Q})Z^{-2} + 2(\frac{\omega_0^2T^2}{4} - 1)Z^{-1} + (1 + \frac{\omega_0T}{2Q} + \frac{\omega_0^2T^2}{4})}$$

In active filters for designing second-order bandpass filter, commonly the circuit with two Op-Amps is used (Zade, 2008). It is more versatile and has a high quality factor and also used in many communication systems. To achieve low power consumption and input referred noise, single Op-Amp filter is used instead of the filter which uses two Op-Amps. In Figure 1 the signal flow graph diagram of the proposed circuit is shown.

![Signal Flow Graph Diagram](image)

Figure 1. Second-Order Single Op-Amp Filter SFG.

The transfer function of this filter is:

$$\frac{V_{out}}{V_{in}} = -\frac{1}{Z_1} \left[ \frac{Z_3}{Z_5} \left( \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_4} \right) + \frac{1}{Z_4} \right]^{-1}$$

where $Z_1 = C_1(1-Z^{-1})$, $Z_2 = C_2(1+Z^{-1})$, $Z_3 = C_3(1+Z^{-1})$, $Z_4 = C_4(1+Z^{-1})$, $Z_5 = C_5(1-Z^{-1})$.

For creating second-order transfer function, the designed circuit is shown in Figure 2:
Instead of resistors, the equivalent circuits which are shown in Figure 3 are replaced.

As one Op-Amp is used, power consumption is reduced to 0.58nW, which is an advantage in fabrication of integrated circuits. With the use of positive feedback in the input stage of the amplifier, power is saved more to enhance its transconductance and control the bias current. The Z-domain transfer function of this filter is:

\[
\frac{-C_3}{C_5} \frac{1}{1-Z^{-2}}
\]

Comparing (3) and (5) all capacitors are computed as:

\[
C_2 = \frac{\omega T}{2Q} \left( C_1 - H_0 C_5 + C_1 \frac{Q^2}{H_0} \right)
\]

\[
C_3 = C_5 H_0 \left( \frac{\omega T}{2Q} \right)
\]

\[
C_4 = C_1 \frac{\omega T Q}{2H_0}
\]

where Q, T, H_0, \omega_0 are known values. There are two degrees of freedom. By choosing the best value for size of C_1 and C_5, size of capacitors C_2, C_3 and C_4 are determined.

Non overlapping clocks are extremely important which applied to switched capacitor filters (Gupta, 2010). These clocks control charge transferring by turning on and off the switches. Clock frequencies should be higher than twice of signal frequency (f_{clock} > 2f_{signal}) (Al-Badawy et al., 2009). This condition should be established to prevent generating of unwanted frequencies so desired bandpass response is produced (Pan et al., 2011). Such unwanted frequencies decrease the dynamic range of filter.

Finite dc gain of Op-Amp cause the gain error that is proportional to 1/A_v and A_v is the gain of Op-Amp (Zhu-Ping et al., 2010). Choosing high gain Op-Amp, solves this drawback. Op-Amp should have low DC offset to achieve minimum signal-to- noise and distortion ratio (Maheshwari and Serdijn, 2009). Low- threshold transistors are used in SC filters as switches to ensure that input and output signal range of Op-Amp is wide enough (Suzuki et al., 2010). NMOS transistors have the low leakage and they also transmit even low voltages (Darfeuille et al., 2006). Moreover,
the mobility of electron is higher than hole. However PMOS transistors have less 1/f noise than NMOS transistors but NMOS transistors are used instead of PMOS in the integrated circuit, because they occupy low area (Lee et al., 2010).

**Improvement Of Quality Factor**

For voice and video signal filtering and other communication circuits which need high quality factor, bandpass filter with two Op-Amps is ideal (Zade, 2008). Increasing quality factor in one Op-Amp bandpass filter needs more analysis. To reach the goal of high maximum gain and quality factor, relationship between these factors and size of capacitors should be extracted. From (6), (7) and (8), maximum gain ($H_0$), center frequency ($f_0$) and quality factor ($Q$) can be expressed as:

\[ H_0 = \frac{C_1C_3}{C_5(C_3+C_4+C_5)} \]  
\[ f_0 = \frac{1}{\pi T} \sqrt{\frac{C_3C_4}{C_1C_5}} \]  
\[ Q = \frac{\sqrt{C_1C_3C_4/C_5}}{C_3+C_4+C_2} \]

It is clear that size of capacitor $C_2$ effect on maximum gain and quality factor without changing center frequency. By decreasing capacitance of $C_2$, different $Q$ and $H_0$ are produced. In (Al-Badawy et al., 2009; Darfeuille et al., 2006) quality- factor tuning technique was proposed and overcomes low quality factor problem. For changing capacitance of $C_2$ different methods are presented. In one of them, clock signal with different frequency is applied to capacitor $C_2$, and change the period which $C_2$ is active during it. Therefore (9), (10) and (11) are changed as follows:

\[ H_0 = \frac{C_1C_3}{C_5(C_3+C_4+(\frac{pq}{m})C_2)} \]  
\[ f_0 = \frac{1}{\pi T} \sqrt{\frac{C_3C_4}{C_1C_5}} \]  
\[ Q = \frac{\sqrt{C_1C_3C_4/C_5}}{C_3+C_4+(\frac{pq}{m})C_2} \]

where $pq$ is the number of pulses and $m$ is the number of cycles. Factor $\frac{pq}{m}$ in (12) and (14) controls the maximum gain and the quality factor’s range without any changes in central frequency. Therefore the number of pulses, rise time, fall time and clock frequencies are very important in determining characteristics of switched capacitor filter. In Table 1 some of the information about clock signals is summarized. $S_{C2}, S_{C3}$ and $S_{C4}$ relate to the switches around capacitors $C_2, C_3$ and $C_4$ which organize equivalent bilinear resistors.

<table>
<thead>
<tr>
<th>Table 1. Cock signals characteristics</th>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{C2}$</td>
<td>Rise time</td>
<td>100 µs</td>
</tr>
<tr>
<td></td>
<td>Fall time</td>
<td>100 µs</td>
</tr>
<tr>
<td></td>
<td>Amplitude</td>
<td>1.2 V</td>
</tr>
<tr>
<td></td>
<td>Rise time</td>
<td>200 µs</td>
</tr>
<tr>
<td>$S_{C3}$</td>
<td>Fall time</td>
<td>200 µs</td>
</tr>
<tr>
<td></td>
<td>Amplitude</td>
<td>1.2 V</td>
</tr>
<tr>
<td></td>
<td>Rise time</td>
<td>200 µs</td>
</tr>
<tr>
<td>$S_{C4}$</td>
<td>Fall time</td>
<td>200 µs</td>
</tr>
<tr>
<td></td>
<td>Amplitude</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>
RESULTS

A second-order bandpass filter is designed in 0.18 µm CMOS technology. Ideal Op-Amp is used to eliminate gain error of switched capacitor filter. Non overlapping clock generators are applied to each switch. The clock signals have the amplitude of 1.2 volt and the period of all clock signals is 1msec. The non-overlapping clock signals are shown in Figure 4.

![Non-Overlapping Clock Signals](image)

NMOS transistors which are used as switches play an important role in waveform of output voltage. The designing of this switched capacitor filter is based on minimum size of transistors. Therefore $W/L$ for all transistors is determined to 0.3µm/0.18µm. Table 2 shows the characteristics of the capacitors which are really effects on the operation of the switched capacitor filter.

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>$C_3$</th>
<th>$C_4$</th>
<th>$C_5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value (fF)</td>
<td>100</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>30</td>
</tr>
</tbody>
</table>

Figure 5 and Figure 6 shows the frequency response and the output voltage respectively, which are also in agreement with each other. It is clear that capacitors charge and discharge by on and off switches and also they follow input signal.
The layout of the proposed capacitor filter is shown in Figure 7. As it has one Op-Amp, chip area is decreased to 226µm². NMOS Op-Amp is used in the design with different W/L ratios of NMOS transistors. In targeted layout compensation capacitors are considered off chip. The input transistors of the Op-Amp have high W/L ratio in order to achieve high gain, but the biasing transistors of the input stage have long channel, therefore their W/L ratios are smaller than the input transistors.

Some of the transistors which are used as the active loads are depletion-mode devices. By using this technique, the voltage gain of the amplifier is highly increased. The size and the other characteristics of the transistors which are used in the Op-Amp are mentioned in (Grebene, 2003). The other transistors which are designed to work as switches have the same size. It should be noted that the Op-Amp occupy more area in the chip. From the layout, it is really understood that the chip area of each op-Amp is about 141 µm². So by omitting one Op-Amp, chip area is diminished about 38%.

By changing the voltage between source and substrate of the transistors, the threshold voltage of transistors is varied. This variation leads to body effect. For preventing body effect, the body of the transistors in the layout is connected to the ground of the circuit. The capacitors are designed in the range of femto Farad to achieve low chip area. Because NMOS technology is used in the design, the NMOS capacitors are chosen to follow the design.
The quality factor is 0.54 and the maximum gain is 6.8dB. At 1.2 V supply voltage, center frequency of the filter is 300Hz. By using one Op-Amp power consumption decrease into 0.58nW. Table 3 summarizes the characteristics of designed filter and compares it with the other switched capacitor filters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>supply voltage (V)</th>
<th>Quality factor</th>
<th>Central frequency</th>
<th>Clock frequency rate</th>
<th>Power consumption</th>
<th>Chip area</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Lee et al., 2008)</td>
<td>0.9</td>
<td>0.235</td>
<td>1.118 KHz</td>
<td>125 KHz</td>
<td>262 µW</td>
<td>0.35 mm²</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>(Zade, 2008)</td>
<td>1.5</td>
<td>0.35</td>
<td>50 Hz</td>
<td>1024 Hz</td>
<td>210 nW</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Lee et al., 2010)</td>
<td>1.6</td>
<td>-</td>
<td>1 KHz</td>
<td>100 KSample/s</td>
<td>69 µW</td>
<td>6512 µm²</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>This work</td>
<td>1.2</td>
<td>0.54</td>
<td>300 Hz</td>
<td>1 KHz</td>
<td>0.58 nW</td>
<td>226 µm²</td>
<td>0.18 µm</td>
</tr>
</tbody>
</table>

**CONCLUSION**

Second-order switched capacitor filter with a single operational amplifier was proposed in a standard 0.18µm CMOS technology. By using one Op-Amp this structure has low power consumption and low chip area. Tuning technique was used for increasing quality factor. With a central frequency of 300Hz the quality factor is 0.54. The chip area is 226µm² from a 1.2 V supply voltage. The power consumption is measured about 0.58nW, which was shown that the utilized techniques are efficient.

**REFERENCES**


Lee SC, Lee SY, Chiang CH. 2008. 0.9 V low-power switched-opamp switched-capacitor bandpass filter for electroneurography acquisition systems. IEEE IET Circuits Devices Syst, 2: 257-263.


